Physical/Electromagnetic pHEMT Modeling

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***Abstract*—An effective technique, which is based only on geometrical and physical data, is presented for the analysis of high-frequency FETs. The intrinsic part of this electron device is described by a quasi-two-dimensional hydrodynamic transport model, coupled to a numerical electromagnetic field time domain solver in three dimensions that analyzes the passive part of the FET. Such an analysis is entirely performed in the time domain, thus allowing linear and nonlinear operations. The obtained data give insights to some parameters affecting the signal distribution through the entire device structure; a comprehensive discussion of these is given for a test device. In order to prove the validity of the approach, the bias-dependent small-signal analysis is compared with the corresponding measurements up to 50 GHz for two 0.3-μm gate-length AlGaAs–InGaAs–GaAs pseudomorphic high electron-mobility transistors, each having two gate fingers of 25-μm and 100-μm width, at bias points ranging from $Idss$ to the pinchoff regime. The accuracy and the efficiency of the approach make it suitable for device optimization.**

***Index Terms*—Electron device modeling, global modeling, microwave monolithic integrated circuit, pseudomorphic high electron-mobility transistors (pHEMT).**

I. Introduction

THE design of electron devices for microwave and millimeter-wave frequencies is traditionally based upon simple models and basic concepts that are accurate and comprehensive, but use very slow simulators [1]–[4]. These models have become more complex due to the decreasing trend in the device size that has characterized the most recent developments. The actual device geometry (the structure of the electrodes and passive connecting parts) also influences the device characteristics and, hence, may constitute a set of available design parameters. The topology of the passive connecting parts is basically designed by means of cut-and-try procedures; the experience and expertise of the designer is an essential part of this process. For very high frequencies and more advanced devices, this procedure tends to be progressively less effective. Moreover, the growing interest for *a priori* design methods has driven the research effort toward a possibly complete, physical-based approach. The statistical significance and predictive ability are regarded as interesting features for this class of models. It is significant to consider in a self-consistent way the constitutive equations which rule the phenomena appearing in a real electron device. This effort may be accomplished by solving the models for the electromagnetic (EM) field coupling, the carrier transport, and the thermal propagation.

Recently, the research efforts in this field have been broadly termed as global modeling [5]–[17]. The present paper is intended to be a contribution to this fast growing area, where a 0.3-μm pseudomorphic high electron-mobility transistor (pHEMT) is analyzed for low-noise applications. In the present approach, the thermal processes are neglected.

Recent advances in the construction methods have led to devices having typical dimensions of the order of a particle wavelength. As a direct consequence, the quantum mechanics of the particle in such a structure must be properly considered in the phenomena to be modeled, thus increasing the complexity of the description from both the theoretical and numerical points of view. In the case under investigation, a calculation of the two-dimensional electron gas (2DEG) properties must be accounted for; improper estimation leads to a wrong transconductance value and an inexact pinchoff regime. This consideration is even more relevant in the device optimization stage, where the active layer of the transistor can be regarded as a degree of freedom for the designer.

The goal of the present approach is to consider the above described phenomena which self-consistently contribute to the electron device behavior, in a simple but reliable quasi-three-dimensional time-domain description.

The electron device is assumed to consist of an "*extrinsic passive structure*" connected with a finite, suitable number of elementary "*intrinsic devices.*" The intrinsic device analysis considers two models: the first part is the channel charge control which acts in the vertical direction; the second is the electron channel transport in the horizontal direction. The evaluation of these two effects is obtained on the basis of the voltages at the intrinsic device terminals. As a result, a set of currents characterizes the dynamic response of the intrinsic device that is then coupled to a tri-dimensional EM field solver in order to account for the extrinsic passive structure. In turn, the solution for the EM fields gives the time- and space-dependent control voltages at any intrinsic devices.

Several techniques have already been proposed which are based on different approaches and with varying degrees of accuracy and complexity [6]–[11], [15]–[17]. This paper proposes a comparatively simple code which runs on a PC, thus allowing the designer to predict the device behavior and, potentially, to optimize its performance with a reasonable degree of accuracy and affordable computational time [16].

The organization of this paper is as follows. The description of the quasi-bidimensional (Q2D) pHEMT intrinsic region model [1]–[4], [18]–[23], which is composed of two main parts—the approximate nonstationary charge-transport model

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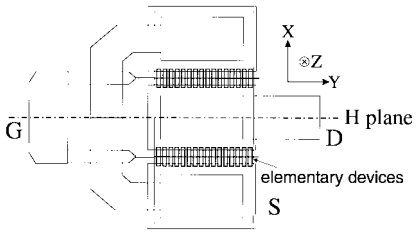


Fig. 1. Structure of the physical/EM FET model.

based on the energy and momentum balance equations and the charge-control model—is presented in Section II. Insights of the most important parameters are given for a test device. The important assumptions on the device operation are introduced in Section III. These enable a strongly simplified link between the Q2D model and the three-dimensional (3-D) EM full-wave model. Finally, small-signal experimental results at microwave frequencies for a 0.3-μm AlGaAs–InGaAs–GaAs pHEMT are presented in Section IV. These confirm the simulation capabilities.

II. Intrinsic pHEMT Physical Model

Fig. 1 shows the schematic representation of a microwave FET where the active part is divided into a convenient number of intrinsic devices. These are analyzed by means of two models: the first is the channel charge control model which operates in the z-direction and the second is the electron channel transport model in the x-direction.

A. Charge-Control Model

The charge-control model of the pHEMT is derived from a self-consistent solution of the Poisson and Schrödinger equations. In this way, it is possible to provide the actual charge-control law as a function of the device layer structure and material composition. This procedure is executed before the calculation of the dynamic behavior, then inserted in the transport calculation by means of a lookup table (LUT) or fitting equation. Hence, the exact description of the 2DEG in the device channel, as a function of the gate-to-channel voltage ($V_{\rm GC}$), is accounted for in a numerically efficient way.

The steady-state Schrödinger's equation is

$$\frac{-\hbar^2}{2m_o}\frac{d}{dz}\left[\frac{1}{m_z^*}\frac{d\psi_i(z)}{dz}\right]+qV_C(z)\psi_i(z)=E_i\psi_i(z) \qquad (1)$$

where m_z^* is the effective mass and E_i and $\psi_i(z)$ are the energy level and the envelope function of the ith subband, respectively. The electrostatic potential is numerically given by the solution of the Poisson's equation

$$\frac{d}{dz}\left[\varepsilon(z)\cdot\frac{dV(z)}{dz}\right]=q\left[N_D^+(z)-n_g(z)\right] \qquad (2)$$

where $V_{(z)}$ is the electrostatic potential through the semiconductor,[1] $\varepsilon(z)$ is the position-dependent dielectric constant, and $N_D^+(z)$ is the ionized donor density. Since the charge density on the right-hand side of (2) depends on the potential variation, an iterative calculation is required. The electron concentration $n_g(z)$ is described as a sum of two contributions: the 2DEG density localized in the channel $n_{\rm 2DEG}(z)$ and the bulk semiconductor electron density localized in the supply layer $n_B(z)$. The first is calculated as described in [24], while the latter is calculated by using the classical model based on 3-D Fermi statistics in which the subband structure is neglected.

In this model, the electrostatic potential $V(z)$ is modified by the conduction band discontinuities ΔE_i at any ith heterointerface. This leads to the definition of the position-dependent conduction band potential

$$V_C(z)=V(z)-\frac{\Delta E_1}{q}u(z-z_1)-\frac{\Delta E_2}{q}u(z-z_2) \qquad (3)$$

which is the potential to be used for the numerical solution of (1). The gate bias dependence of $n_g(z)$ is calculated under the following boundary conditions. The conduction band edge at the gate electrode is determined by the sum of the Schottky-barrier height and the gate voltage. The conduction band edge at a point sufficiently far from the channel is fixed to its thermal equilibrium value. The channel is assumed to be grounded ($V_{\rm gs}$ equal to zero) and the Fermi level fixed to zero. The envelope functions at both boundaries are fixed to be zero.

B. The Nonstationary Charge Transport Model

The electron transport in the channel layer which is assumed to take place essentially in the direction from the source to the drain electrodes (x-direction) is modeled by the Energy and Momentum Balance equations [1]

$$\begin{aligned}\frac{\partial n}{\partial t}&=0\\ \frac{\partial v}{\partial t}&=\frac{qE_x}{m^*}-\frac{v}{\tau_p}\\ \frac{\partial w}{\partial t}&=qvE_x-\frac{w-w_0}{\tau_w}\end{aligned} \qquad (4)$$

where n is the electron density, v is the electron velocity, E_x is the longitudinal electric field, and w is the electron energy, and the relaxation terms τ_p and τ_w as well as w_0 are obtained by steady-state Monte Carlo analysis [25]. The equations are solved in the time domain and account for transient and nonlinear behavior, while the boundary condition is given by time-dependent drain–source voltage. The insertion of the channel control model is obtained from Poisson's equation in the channel

$$\frac{\partial E_x}{\partial x}=\frac{q}{\varepsilon}\left[n-\frac{1}{H}\int_0^h n_g[z,\,V_{\rm sur}-V_{\rm ch}]\cdot dz\right] \qquad (5)$$

where H is the device thickness and ε is the dielectric constant. The voltages $V_{\rm sur}(x,\,t)$ and $V_{\rm ch}(x,\,t)$ represent the air–semiconductor and channel voltages, respectively. The gate- and drain-bias dependences of n and v are calculated under the following boundary conditions. The potentials $V_{\rm sur}(t)$ and $V_{\rm ch}(t)$ are fixed to zero at the source terminal and equal to $V_{\rm ds}(t)$ at the drain terminal. At the gate electrode, $V_{\rm sur}(t)$ is fixed to the sum of the Schottky-barrier height and the time-dependent gate

[1]This potential corresponds to the modification of the vacuum level through the semiconductor.

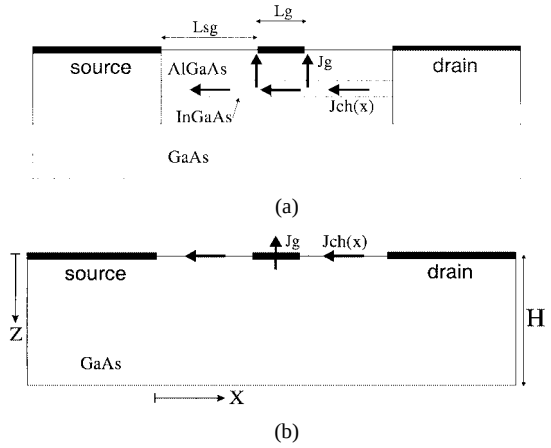


Fig. 2. (a) Schematic representation of the intrinsic device cross section. (b) Model for the EM solver. Design not to scale.

voltage $V_{\rm gs}(t)$. The solution of the system (4) together with (5) allows the channel current density $J_{\rm ch}(t)$ to be calculated. A proper estimation of the conduction dynamic gate current Jg, as well as of the displacement current due to geometric capacitances associated with the electrodes, is required to evaluate the device input impedance and its gain. In the model proposed, this is accounted for by the EM analysis, while the following relation calculates the gate junction current component:

$$Jg(t) = qn(t) \cdot v(t)|_{x=L\rm sg} - qn(t) \cdot v(t)|_{x=L\rm sg+Lg} \qquad (6)$$

where Lsg is the gate-to-source spacing and Lg is the gate length [see Fig. 2(a)].

III. EM Electron Transport Model Coupling Technique

In a microwave FET, the thickness of the active layer (usually less than 0.1 μm) is much smaller than the total thickness of the device, usually on the order of tens to hundreds of micrometers [4], [see Fig. 2(a)]. An infinitely thin layer can therefore represent the active region when solving for the EM field in the whole structure [16]. This layer has obviously an active behavior and is represented by nonlinear distributed voltage-controlled current sources to be included in the model of the passive structure [see Fig. 2(b)]. It extends in the horizontal plane between the source and drain electrodes and all along the gatewidth. It is worth noting that for the EM problem such an assumption allows a strong reduction in the computational effort through a less severe space discretization in the z-direction, as is otherwise necessary [17], thus making this approach suitable for an efficient analysis of real electron devices. The EM-wave propagation is completely characterized by solving the Maxwell's equations in the time domain by using a 3-D mesh. The equations are solved in the time domain with the conventional iterative scheme [26].

The active region is represented by controlled current sources: $J_{\rm ch}(x, y)$ at the interface between air and semiconductor and $J_g(y)$ placed in the middle of the gate contact in the z-direction. The controlled currents are a function of the gate–source and gate–drain current via the transport equations and are intrinsically nonlinear; the equations at each time step must be solved iteratively by means of Newton's algorithm.

The insertion of such a contribution is obtained through the Maxwell's curl $\overline{H}$ equations, as discussed in [26]

$$E_x|_{i,j,k}^{N+1} = E_x|_{i,j,k}^{N} + \frac{\Delta t}{\varepsilon} \nabla \times H|_{i,j,k}^{N+1/2} - \frac{\Delta t}{\varepsilon} J_{ch}|_{i,j}^{N+1/2}$$
$$E_z|_{i,j,k}^{N+1} = E_z|_{i,j,k}^{N} + \frac{\Delta t}{\varepsilon} \nabla \times H|_{i,j,k}^{N+1/2} - \frac{\Delta t}{\varepsilon} J_g|_{j}^{N+1/2}. \qquad (7)$$

The schematic representation for the channel and gate currents for an elementary device is shown in Fig. 2(b).

For comparison with experimental data, an input signal is applied as a sinusoidal electric field source with a 50-Ω impedance at the input of the device, i.e., at the gate side, while a 50-Ω load resistance is placed at the output, i.e., at the drain side of the device.

The outline of the actual simulation process is as follows.

Step 0) The bias voltages Vgs and Vgs are supplied to any intrinsic region and the static channel and gate currents are evaluated.

Step 1) The dynamic simulation begins and the electric and magnetic field distributions are calculated in all the space at the time steps $N\Delta t$ and $(N + 1/2)\Delta t$, respectively, as the result of the input signal.

Step 2) The electric field x component is extrapolated at the time step $(N + 1/2)\Delta t$ on the basis of its value assumed in the previous time steps. The potentials $V_{\rm ds}(y)$ and $V_{\rm gs}(y)$ are then calculated by using

$$V_{is}(y) = -\int_{\rm source}^{\rm conductor\ i} \overline{E}(y) \cdot d\overline{S}. \qquad (8)$$

Step 3) $V_{\rm ds}$ and $V_{\rm gs}$ are added to their relative static components and used to solve the electron transport model.

Step 4) The electric field, which is effectively defined at $(N + 1)\Delta t$, is calculated by using (7) and the currents obtained at the previous step.

Step 5) The magnetic field is evaluated at the step $(N + 3/2)\Delta t$.

Steps 1)–5) are repeated until the entire period of interest is exploited.

IV. Experimental Results

The technique proposed has been applied to two pHEMTs manufactured by AMS Alenia–Marconi System. The active layer structure is given in Table I, and the other parameters of interest are: the source–gate and gate–drain distances Lsg $= L$gd $= 1.2$ μm and gate length $Lg = 0.3$ μm; the devices have two gate fingers with a gatewidth of 25 and 100 μm, respectively. With reference to Fig. 1, the grid for the definition of the geometry is: $\Delta x = 0.15$ μm, $\Delta y = 5$ μm, $\Delta z = 10$ μm, while the time stepping Δt is 10^{-15} s in order to prevent numerical instability. The analysis involves

TABLE I
SUMMARY OF THE PHEMT LAYER STRUCTURE

Layer Function	Structure	Thickness [Å]	Dopant [cm^{-3}]	Al or In content
Cap Layer	GaAs: Si	1200	3.5E18	-
1st supply layer	AlGaAs: Si	300	1.0E17	0.22
2nd supply layer	AlGaAs: Si	150	2.0E18	0.22
Spacer	AlGaAs	20	-	0.22
Channel	InGaAs	130	-	0.15
Buffer layer	GaAs	5500	-	-
S.I. substrate	GaAs	1E6	-	-

TABLE II
PHYSICAL PARAMETERS USED FOR CHARGE CONTROL CALCULATIONS

Parameter	$Al_{0.3}Ga_{0.7}As$	$In_{0.15}Ga_{0.85}As$	GaAs
band gap [eV]	1.814	1.220	1.439
electron effective mass	0.089	0.063	0.063
light-hole effective mass	0.084	0.076	0.085
heavy-hole effective mass	0.450	0.444	0.410
conduction band density of states at 300K [cm^{-3}]	6.988E17	4.043E17	4.350E17
valence band density of states at 300K [cm^{-3}]	9.313E18	9.588E18	9.985E18
relative dielectric constant	12.1	13.4	13.1

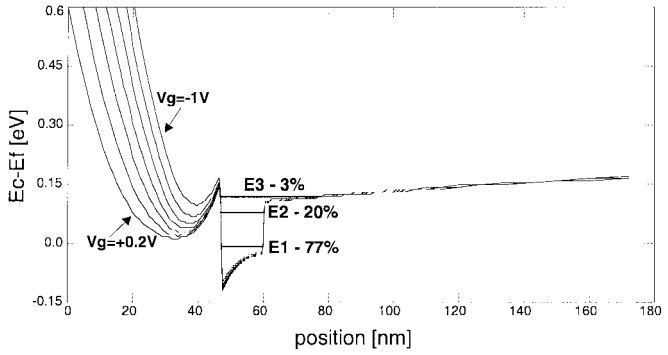


Fig. 3. Band energy diagram calculated for a gate bias voltage $V_{\rm gs}$ ranging from -1 to $+0.2$ V, with 0.2-V steps and $V_{\rm ds} = 0$ V.

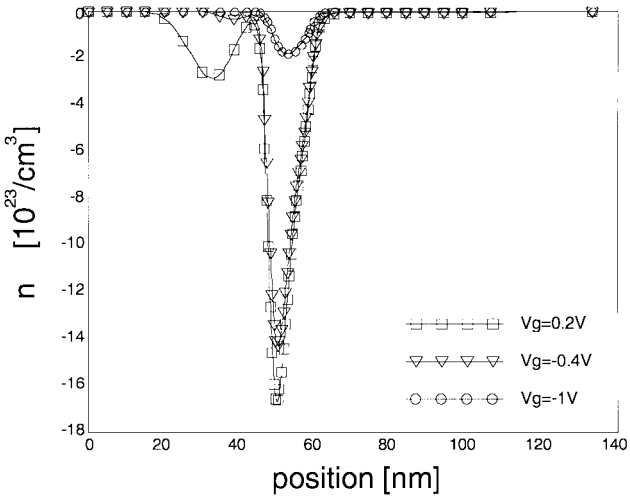


Fig. 4. Total charge density calculated for a gate bias voltage $V_{\rm gs}$ ranging from -1 to 0.2 V, with $V_{\rm ds} = 0$ V.

a longitudinal perfect magnetic wall to reduce the simulation domain (see Fig. 1).

A. Intrinsic Physical Results

The analysis begins with the calculation of the charge distribution in the pHEMT active area by using the charge-control model described in Section II-A. The physical parameters used in the present paper are listed in Table II. It is assumed that the conduction band edge discontinuities at the heterointerfaces are 85 percent of the bandgap discontinuity as in [24].

Fig. 3 shows the calculated conduction band profile for a gate bias voltage ranging from -1 to $+0.2$ V. The induction of a 2DEG system in the InGaAs channel is confirmed; the calculation allows the subband levels to be evaluated and their fractional occupation. For the case under investigation, $E1 = -1.84$ meV, $E2 = 75$ meV, and $E3 = 91.2$ meV with corresponding probabilities of occupation of 77%, 20%, and 3%, respectively. From this calculation, it is possible to observe that only the first two subband energy levels give a contribution to the channel electron density, while $E3$ and higher levels are empty of charge.

Although not reported here, subbands are also formed in the supply and spacer layers, their energy distribution being very sensitive to the bias voltage and responsible for the well-known MESFET-like parasitic channel. The energy diagram shows a flat-band behavior in the buffer layer and the semi-insulating substrate; hence, the component of the electric field E_Z is equal to zero.

Fig. 4 reports the corresponding total charge density distribution profile in the semiconductor structure including the ionized donor atoms and the electrons in the conduction band, for the gate potential ranging from -1 to $+0.2$ V, with the drain and source potentials kept to zero. The graph shows that the charge distribution vanishes for a distance from the gate electrode larger than 70 nm. This means that any electron flow through the substrate during the dynamic operation is only due to displacement currents, while conduction currents are

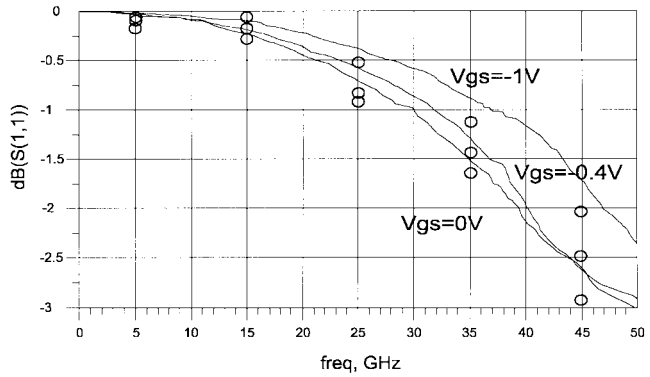


Fig. 5. Comparison between simulated (symbols) and measured (solid lines) $S11$ for $V_{\rm ds} = 3$ V and different gate bias for the $2 \times 25\ \mu$m gatewidth pHEMT.

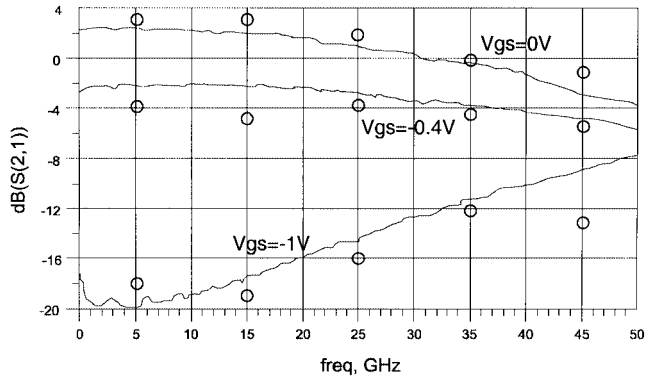


Fig. 6. Comparison between simulated (symbols) and measured (solid lines) $S21$ for $V_{\rm ds} = 3$ V and different gate bias for the $2 \times 25\ \mu$m gatewidth HEMT.

not allowed. Consequently, the assumption made in Section III is consistent with the device physics.

The charge control model presented above has been implemented by using a finite difference one-dimensional (1-D) spatial mesh and solved by the Gummel method; the results are then made available in terms of an LUT then inserted into the dynamic calculation by using (5).

B. Microwave Results

In order to validate this approach, S-parameters measured and modeled up to 50 GHz are shown in Figs. 5–8 for both the HEMT structures, three gate voltages from open channel to pinchoff, and 3-V drain bias voltage. In order to compare the results of the analysis with the device performance, the actual device layout is considered which includes the in–out transmission lines and the ground–signal–ground (G–S–G) contact pads. The analysis is performed entirely in the time domain, and linear and nonlinear operations of this device are allowed. Postprocessing of the data provides a deep insight into the device dynamics and the small-signal results at microwave and millimeter-wave frequencies.

The analysis of the $2 \times 25\ \mu$m transistor has been performed in two separated steps, first by feeding from the gate terminal, then from the drain terminal and sensing the reflected and the transmitted signals. The incoming signal (a_1- and a_2-parameters) have been supplied through a 50-Ω impedance by using the technique described in [27], while the calculation of the

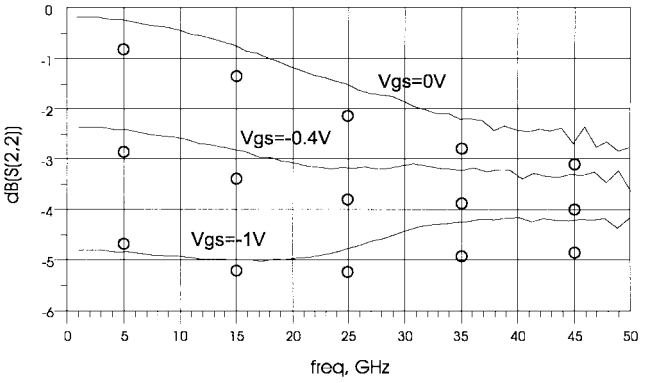


Fig. 7. Comparison between simulated (symbols) and measured (solid lines) $S22$ for $V_{\rm ds} = 3$ V and different gate bias for the $2 \times 25\ \mu$m gatewidth pHEMT.

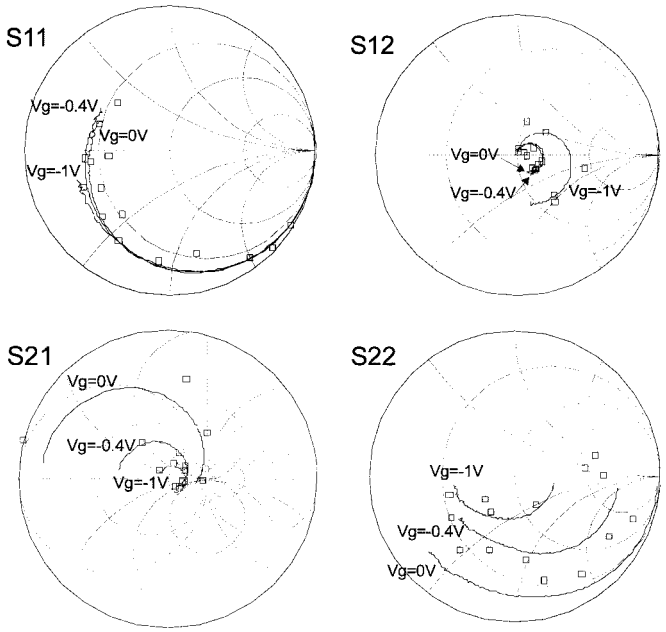


Fig. 8. Comparison between simulated (symbols) and measured (solid lines) $S22$ for $V_{\rm ds} = 3$ V and different gate bias for the 100-μm gatewidth HEMT; the simulation points are 5–45 GHz in 10-GHz steps.

b_1- and b_2-parameters is obtained in the same way as that of measuring the voltage for a lumped resistor. This has allowed the calculation of the magnitude for $S11$, $S21$, and $S22$ reported in Figs. 5–7, respectively, while the corresponding phase responses are reported in terms of percent relative errors in Table III. Finally the same comparison is reported in Table IV for the $S12$-parameter.

In order to test the actual model capability, the $2 \times 100\ \mu$m device has been modeled and the results compared with corresponding measurements. The transistor has exactly the same semiconductor structure and was conceived by applying the same design rules; the only change with respect to the previous device is the gatewidth. In that case, the EM effects would be more significant. The comparisons between measurement and simulation, up to 50 GHz, are reported in Fig. 8. From the graphs reporting $S21$ for both the pHEMTs, Figs. 6 and 8(c), it is possible to note that the gate voltage of the data measured is actually shifted by 0.2 V with respect to the simulated data; this data is easily estimated by the $Id\backslash Vg$ graph reported in

TABLE III
$S11$, $S21$, AND $S22$ PHASE PERCENT ERROR AT DIFFERENT GATE BIASES AND FREQUENCIES FOR THE 2×25 GATEWIDTH pHEMT

Freq	Phase (S11)			Phase (S21)			Phase (S22)		
	Vg=0V	Vg=-.4V	Vg=-1V	Vg=0V	Vg=-.4V	Vg=-1V	Vg=0V	Vg=-.4V	Vg=-1V
5GHz	-1.0E1	2.4E1	-8.6E1	7.4	-1,4E1	-2.8E1	-2.3E1	-1E1	-0.2
25GHz	-1.3E1	1.3E1	-2.0E1	-3.7E1	3.8	-3.4E2	-1.7E1	-1.0E1	1.2E1
45GHz	1.3E1	2.0E2	-1.3E1	-6.8E1	2.0E2	3.6E1	1.2E2	1.1E2	1.0E2

TABLE IV
$S12$ PERCENT ERROR AT DIFFERENT GATE BIASES AND FREQUENCIES FOR THE 2×25 GATEWIDTH pHEMT

Freq	Magnitude (S12)			Phase (S12)		
	Vg=0V	Vg=-.4V	Vg=-1V	Vg=0V	Vg=-.4V	Vg=-1V
5GHz	4.4E1	6.8E1	-1.2E2	-34.1	-16.0	-7.2
25GHz	6.4E1	1.1E1	-2.6E1	97.2	-75.2	-63.4
45GHz	2.1E1	-1.2E1	-1.2E1	20.9	20.3	16.5

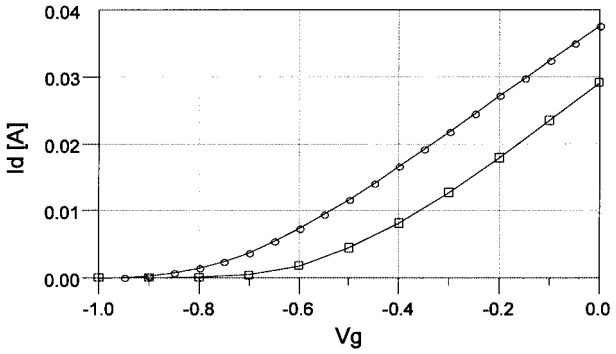


Fig. 9. Comparison between simulated (circle) and measured (square) drain current for $V_{\rm ds}$ =3 V and different gate bias for the 2 × 100 μm gatewidth pHEMT.

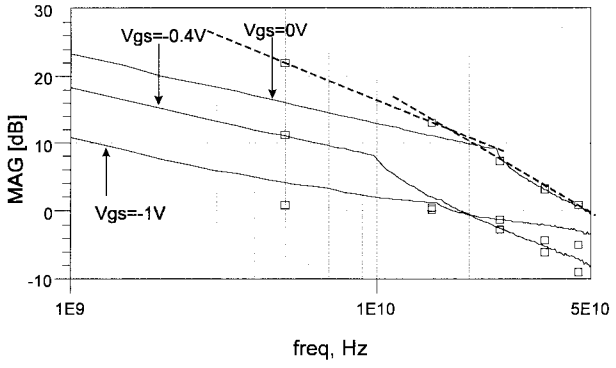


Fig. 10. Comparison between simulated (symbols) and measured (solid) MAG for $V_{\rm ds}$ = 3 V and different gate bias for the 2×100 gatewidth HEMT.

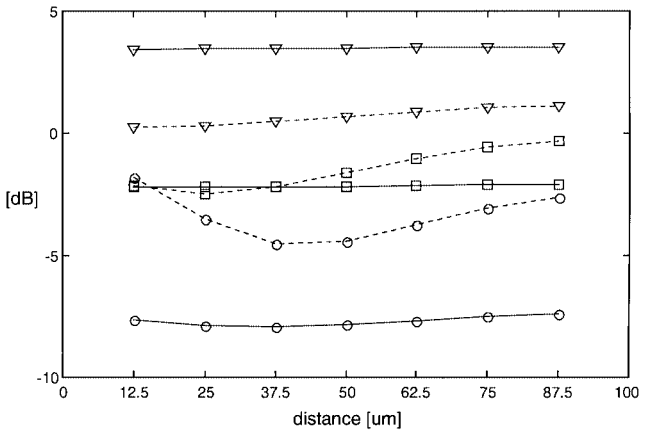


Fig. 11. Signal power distribution through the drain (solid lines) and gate (dashed lines) electrode at 25 GHz (triangle), 50 GHz (square), and 75 GHz (circle). $V_{\rm ds}$ = 3 V and $V_{\rm gs}$ = 0 V.

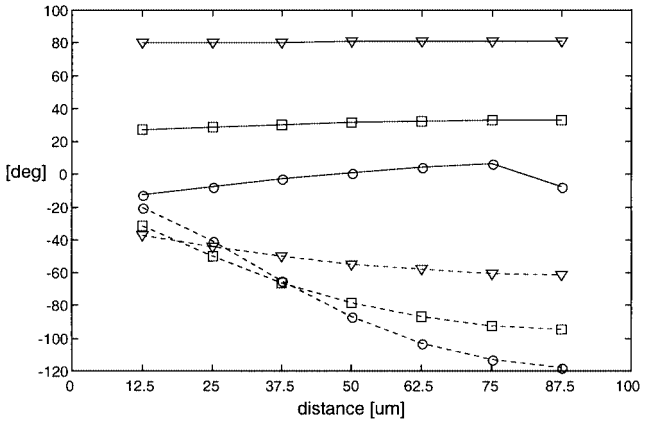
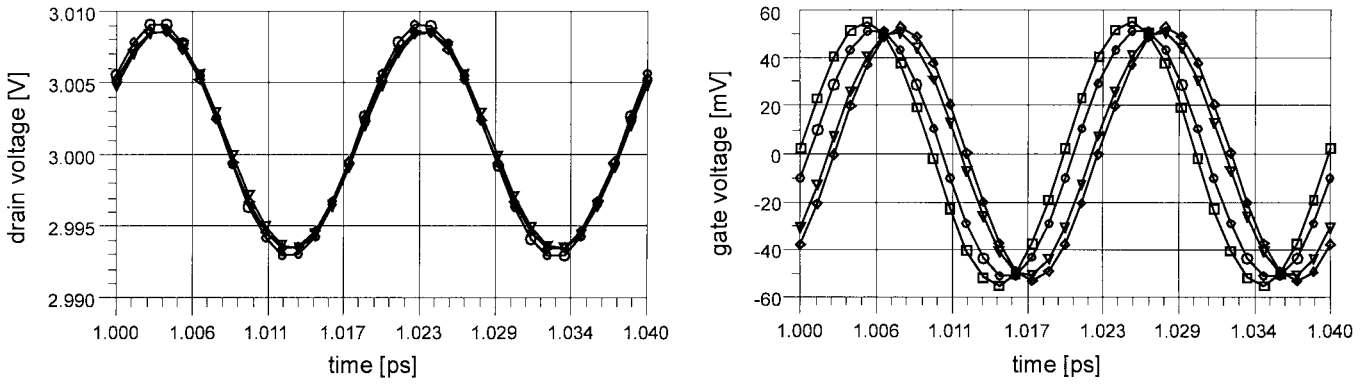


Fig. 12. Signal phase distribution through the drain (solid lines) and gate (dashed lines) electrode at 25 GHz (triangle), 50 GHz (square), and 75 GHz (circle). $V_{\rm ds}$ = 3 V and $V_{\rm gs}$ = 0 V.

Fig. 9 for the 2 × 100 μm device. This is probably due to the uncertainty of the technological process. The shift in the current parameter is also responsible for a fictitious increase in drain current and consequently in a gain increase. The results are otherwise satisfactory and promising for an accurate prediction of the device performance.

The results are also reported in terms of MSG-MAG for this device (see Fig. 10). This latter parameter assumes relevance because it may be used as a device figure-of-merit during the optimization of the device structure itself. From measurements, we see that the frequency limits, below which the transistor becomes potentially unstable, change with the gate potential, as expected. In the case of Vgs = 0 V, we estimate a frequency limit around 20 GHz for both the measured and simulated data.



(a) (b)

Fig. 13. Signal distribution distribution through the: (a) drain and (b) gate electrodes sampled at the following points. Circles: $y = 12.5\,\mu$m. Triangles: $y = 50\,\mu$m. Diamond lines: $y = 87.5\,\mu$m. In (b), the input 50-GHz sinusoidal signal is also reported (squares).

Consequently, the design procedure can be driven by the maximization of this parameter around the operation frequency. Its accuracy depends on the accuracy with which the scattering parameters are predicted; as a result, it may be slightly poorer, although the comparison in Fig. 10 shows a fairly constant prediction over the gate bias voltages.

C. Distributed Effects

The approach described herein allows an insight to the intrinsic device behavior that becomes important during the device design. Besides the electron charge accumulation reported in Fig. 4, it is also interesting to observe the signal distribution through the gate and drain electrodes for the $2 \times 100\ \mu$m device. This calculation is made by considering the integration of the electric field in the x-direction by keeping $z = 0$ (see Figs. 1 and 2). The potential is calculated with respect to the source electrode for y which spans over the whole intrinsic active region. In order to show how the distribution of the input and output signals depend upon the frequency, the calculation is repeated for 25, 50, and 75 GHz for a test input signal of 0 dBm of available power. Fig. 11 reports the difference between the inner gate–source voltages at any intrinsic devices and the input voltage in decibels as a function of the distance from the input, while Fig. 12 depicts the same difference in phase.

At this point, some remarks can be conveniently made. The most important phenomen consists in the signal attentuation between the supply generator and the inner gates; this can be avoided with a matching network. Once the signal is fed through the gate, it is appreciably delayed (dashed line in Fig. 12), but only slightly attenuated when propagating through the electrode (dashed lines in Fig. 11). The phase delay depends upon the frequency and is more noticeable for the gate than for the drain. The attenuation is not very sensitive to the distance from the access point; in particular, the drain voltage is constant through the electrode even though it is strongly dependent on the frequency. This is due to the size of the drain electrode that acts as a reference plan for the drain of the intrinsic devices; a comparable result is not obtained for the gate due to its very narrow width. The nonlinear dependence on the distance of the gate signal magnitude, noticeable at 50 and 75 GHz, is due to the combination of attenuation and feedback which are associated with

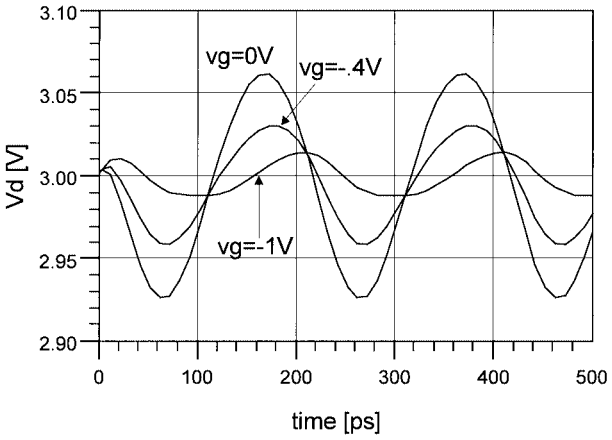


Fig. 14. Internal drain voltages at different gate biases for $V_{ds} = 3$ V bias voltage.

the drain–gate capacitance. For the particular case of 50 GHz, it is also apparent that the magnitude of the drain signal is in excess of the gate signal up to a distance of 37.5 μm; this means that at this frequency the complete device is not efficiently exploited. This result is also consistent with the cut-off frequency calculated from the MAG shown in Fig. 10. It can be concluded that the device should be shortened to a gatewidth of less than 37.5 μm, if intended for an operation frequency of 50 GHz.

The same results in the time domain are reported in Fig. 13 for an input signal of 50 GHz. This approach allows the large-signal model capability [18]–[28]. In Fig. 14, the drain voltage is reported which is sampled in the middle of the gate electrode $y = 50\,\mu$m), as the response to an input signal at 5 GHz 1 V peak to peak. The distortion of the waveform confirms the capability of this technique to deal with a nonlinear regime although a complete discussion of this topic is beyond the aim of this paper.

V. Conclusion

The approach presented herein deals with the problem of global modeling for state-of-the-art pHEMTs operating at frequencies where the EM-field interaction significantly affects the device performance. This technique is based only on geometrical and material data and includes the transport phenomena in the active device, charge control due to quantum

mechanical properties, and the EM interaction between the intrinsic device and the electrodic–dielectric structure of the access elements. The approach proposed in this paper takes advantage of the physically expected assumption that the charge distribution within the intrinsic device could be considered as thin and located near the semiconductor–air interface; the resulting intrinsic device description is more easily inserted into the EM code. This leads to a comparatively very simple code which runs on a PC in a few hours per bias point depending on the platform, thus allowing the designer to predict the behavior of the device and potentially optimizing its performance with a reasonable degree of accuracy and limited computer-time consumption. Although the EM problem has been presently solved by performing a 3-D analysis, this approach allows simplified schemes to be considered like the planar 3-D technique implemented in many commercial tools.[2] In order to validate this technique, the comparison between experimental and simulated small-signal results up to 50 GHz is presented for two gate fingers devices manufactured by Alenia–Marconi with a 25-μm and 100-μm gatewidth, respectively, and a 0.3-μm gate length, at bias points ranging from $Idss$ to the pinchoff regime.

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